CLAIMS

1. A non-volatile memory cell integrated on a semiconductor substrate and comprising:

a floating gate transistor including a source region and a drain region, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region and a control gate region,

characterised in that said floating gate region is insulated laterally, along the width direction, by a dielectric layer with low dielectric constant value.

2. A memory cell according to claim 1, characterised in that said floating gate regions are covered by a dielectric layer before being insulated from each other through said dielectric layer with low dielectric constant value.

3. A memory cell according to claim 1, characterised in that said dielectric layer with low dielectric constant value is bounded between said floating gate regions.

4. A memory cell according to claim 1, characterised in that said dielectric layer with low dielectric constant value is formed by a layer of material having a dielectric constant comprised between 1 and 3.9.

5. A memory cell according to claim 1, characterised in that said dielectric layer with low dielectric constant value is formed by a silicon oxide layer doped for example with fluorine.

6. A memory cell according to claim 1, characterised in that said dielectric layer with low dielectric constant value is formed by a carbon oxide layer hydrated with alkylic groups.

7. A process for manufacturing non-volatile memory cells on a semiconductor substrate organized in rows and columns to form a memory cell matrix, comprising

the following steps:

form active areas in said semiconductor substrate bounded by an insulating layer,

form on said active areas a first dielectric material layer,

deposit a first conductor material layer on said first dielectric material layer,

define through a standard photolithographic technique a plurality of floating gate regions in said first conductor material layer,

characterised in that it comprises the following steps:

form a dielectric layer with low dielectric constant value on said floating gate regions.

8. A process for manufacturing non-volatile memory cells according to claim 7, characterised in that said dielectric layer with low dielectric constant value is bounded between said adjacent floating gate regions belonging to the same row.

9. A process for manufacturing non-volatile memory cells according to claim 7, characterised in that said dielectric layer with low dielectric constant value is deposited through CVD techniques.

10. A process for manufacturing non-volatile memory cells according to claim 7, characterised in that said dielectric layer with low dielectric constant value is deposited through spin on glass techniques.

11. A process for manufacturing non-volatile memory cells according to claim 7, characterised in that said dielectric layer with low dielectric constant value is formed by a layer of material having a dielectric constant comprised between 1 and 3.9.

12. A process for manufacturing non-volatile memory cells according to claim 7, characterised in that said dielectric layer with low dielectric constant value is formed by a silicon oxide layer doped for example with fluorine.

13. A process for manufacturing non-volatile memory cells according to claim 7,

characterised in that said dielectric layer with low dielectric constant value is formed by a carbon oxide layer hydrated with alkylic groups.

14. A process for manufacturing non-volatile memory cells according to claim 7, characterised in that said floating gate regions are covered by a dielectric layer before being insulated from each other through said dielectric layer with low dielectric constant value.

15. A memory cell matrix formed on a semiconductor substrate comprising a plurality of memory cells organized in rows and columns, each cell being formed according to claim 1, the cell matrix being characterised in that adjacent memory cells belonging to a same row of said memory cell matrix are insulated from each other by a dielectric layer with low dielectric constant value.

16. A memory-cell structure formed on a semiconductor substrate, the memory-cell structure comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell structure including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the structure.

17. The memory-cell structure of claim 16 further comprising a dielectric layer having a greater dielectric constant than the insulating regions formed on the floating gate regions.

18. The memory-cell structure of claim 16 wherein the insulating layer has a dielectric constant having a value of between approximately 1 and approximately 3.9.

19. The memory-cell structure of claim 16 each memory cell further comprises a control gate region capacitively coupled to the floating gate region through a dielectric layer having a dielectric constant greater than that of the insulating layer, and wherein the control gate regions of memory cells in respective rows are

electrically interconnected.

20. The memory-cell structure of claim 16 wherein each memory cell comprises a FLASH memory cell.

21. A memory device, comprising:

a memory-cell array formed on a semiconductor substrate, the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell array including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the array.

22. The memory device of claim 21 wherein the memory device comprises a FLASH memory device and each memory cell comprises a FLASH memory cell.

23. The memory device of claim 21 further comprising a dielectric layer having a greater dielectric constant than the insulating regions formed on the floating gate regions.

24. An electronic system, comprising:

a memory device including,

a memory-cell array formed on a semiconductor substrate, the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell array including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the array.

25. The electronic system of claim 24 wherein the electronic system comprises a computer system.

26. The electronic system of claim 25 wherein the memory device comprises a

FLASH memory device and each memory cell comprises a FLASH memory cell.

27. A method of forming an array of memory cells on a semiconductor substrate, the method comprising:

forming a plurality of memory cells on the substrate and arranged in rows and columns, each memory cell including a respective floating gate region; and

forming a first dielectric region between the floating gate regions of adjacent memory cells in respective rows of memory cells, the first dielectric layer having a relatively small dielectric constant.

28. The method of claim 27 further comprising:

forming a second dielectric layer on the floating gate regions, the second dielectric layer having a dielectric constant that is greater than the dielectric constant of the first dielectric layer; and

forming a control gate region for each memory cell on the second dielectric layer adjacent the corresponding floating gate region.

29. The method of claim 27 wherein each first dielectric region has dielectric constant of between approximately 1 and approximately 3.9.

30. The method of claim 29 wherein the each first dielectric region comprises a silicon oxide layer doped with fluorine.